

CALL FOR PAPERS

Workshop on Architecture-aware Simulation and Computing (AASC'09)

As part of the 2009 International Conference on High Performance Computing & Simulation
(HPCS 2009)
and in conjunction with the 5th International Wireless Communications and Mobile
Computing Conference (IWCMC 2009)

Leipzig, Germany
June 21 - 24, 2009

Submission Deadline: February 27, 2009

Background

With multi- and many-core based systems, performance increase on the microprocessor side will continue according to Moore's Law, at least in the near future. However, the already existing performance limitations due to slow memory access are expected to get worse with multiple cores on a chip, and complex hierarchies of cache memory will make it hard for users to fully exploit the theoretically available performance. In addition, the increasingly hybrid and hierarchical design of compute clusters and high-end supercomputers, as well as the use of accelerator components (Cell BE or GPGPUs, e.g.) add further challenges to efficient programming in HPC applications.

Therefore, compute and data intensive tasks can only benefit from the hardware's full potential, if both processor and architecture features are taken into account at all stages – from the early algorithmic design to the final implementation.

Our workshop strives to address all aspects related to these issues, including, but not limited to:

- Hardware-aware, compute- and memory-intensive simulations of real-world problems in computational science and engineering (for example, from applications in electrical, mechanical, civil, or medical engineering).
- Architecture-aware approaches for large-scale parallel simulations in both

implementation and algorithm design, including scalability studies.

- Architecture-aware parallelisation on HPC platforms; esp. platforms with hierarchical communication layout, multi-/many-core platforms, NUMA architectures, or accelerator components (Cell BE, GPU, FPGA).
- Parallelisation with appropriate programming models and tool support for multi-core and hybrid platforms.
- Software engineering, code optimisation, and code generation strategies for parallel systems with multi-core processors.
- Tools for performance and cache behavior analysis (including cache simulation) for parallel systems with multi-core processors.

Paper Submission, Registration, and Publication

You are invited to submit original and unpublished research works on one of the above topics, or on closely related topics in HPC and simulation. Please submit a PDF copy of your full manuscript, not to exceed 7 double-column IEEE formatted pages, and include up to 6 keywords and an abstract of no more than 350 words. Additional pages will be charged additional fee. Instructions for final manuscript format and requirements will be posted on the Conference's web site later. Each paper will receive a minimum of three reviews. At least one of the authors of each accepted paper will have to register and attend the HPCS'09 conference for presenting the paper at the session. Accepted papers will be published in the conference proceedings which will be available at the time of the meeting. Papers should be submitted as PDF files only, and via email to: Michael.Bader@cs.tum.edu. Acknowledgement will be sent within 48 hours of submission.

If you have any questions about paper submission or the session, please contact the session organizers.

Important Dates:

Full Paper Submission Deadline: ----- Feb 27, 2009
Notification of Acceptance: ----- Mar 30, 2009
Camera-Ready papers Due ----- April 24, 2009

Workshop Organizers

Michael Bader

Institut für Informatik - Technische Universität München
Germany

Phone: +49 - 89 - 289 - 1 86 34

Fax: +49 - 89 - 289 - 1 86 07

Email: bader@in.tum.de, Michael.Bader@cs.tum.edu

Josef Weidendorfer

Institut für Informatik - Technische Universität München

Germany

Phone: +49 89 289 18454

Fax: +49 89 289 17662

Email: weidendo@cs.tum.edu

Technical Program Committee:

All submitted papers will be rigorously reviewed by the workshop technical program committee members.

(International Program Committee to be announced shortly.)

If you have any questions about conference paper submission, please contact conference Program Chair: Waleed W. Smari, Dept. of Electrical and Computer Engineering, University of Dayton, 300 College Park, Dayton, OH 45469-0226, USA, Voice: (937) 229-2795, Fax: (937) 229-4529, Email: Waleed.Smari@notes.udayton.edu. For information about the HPCS conference in general, please contact the General Chairs or consult the conference web site at <http://cisedu.us/cis/hpcs/09/main/callForPapers.jsp>.

For information about the IWCMC conference in general, please contact the General Chair: Mohsen Guizani, (Western Michigan University, mguizani@ieee.org). The IWCMC Conference web site is at <http://iwcmc.com/>.