# CALL FOR PAPERS

## Workshop on Architecture-aware Simulation and Computing (AASC'08)

**As part of the 2008 International Conference on High Performance Computing & Simulation (HPCS 2008)
and in conjunction with the 22nd European Conference on Modeling and Simulation (ECMS 2008)**

**Nicosia, Cyprus
June 3 - 6, 2008**

## Submission Deadline: March 15, 2008

### Background

With multi- and many-core based systems, performance increase on the microprocessor side will continue according to Moore's Law, at least in the near future. However, the already limited memory access is expected to get worse with multiple cores on a chip, and gets more complex because of the required hierarchies of cache memory. In addition, the increasingly hybrid and hierarchical design of high-end systems, including accelerator components, is another obstacle for programming. All mentioned issues will have a major impact on overall performance in future systems.

This means that compute and data intensive tasks can only benefit from the hardware's full potential if both processor and architecture features are taken into account at all stages – from the early algorithmic design to the final implementation.

Areas of interest for workshop submissions include, but are not limited to:

- Hardware-aware, compute- and memory-intensive simulations of real-world problems from electrical, mechanical, civil, or medical engineering requiring parallel simulation techniques.

- Architecture-aware, and particularly multi-core-aware approaches for large-scale parallel simulations in both implementation and algorithm design, including scalability studies.

- Compiler techniques and code optimization strategies for parallel systems with multi-core processors.

- Tools for performance and cache behavior analysis (including cache simulation) for parallel systems with multi-core processors.
- Parallelization with appropriate programming models and tool support for multi-core and hybrid platforms.

## Paper Submission, Registration, and Publication

You are invited to submit original and unpublished research works on above and other topics related to simulation and modeling of multicore and multiprocessing systems. Please submit a PDF copy of your full manuscript, not to exceed 7 double-column IEEE formatted pages, and include up to 6 keywords and an abstract of no more than 350 words. Each paper will receive a minimum of three reviews. At least one of the authors of each accepted paper will have to register and attend the HPCS'08 conference for presenting the paper at the session. Accepted papers will be published by ECMS in the conference proceedings. Papers should be submitted as attachments to: Michael.Bader@cs.tum.edu. If accepted, final papers will follow the format that ECMS follows which will be posted on the web site.

If you have any questions about paper submission or the session, please contact the session organizers.

## <u>Important Dates</u>:

Full Paper Submission Deadline: ------------- **March 15, 2008**
Notification of Acceptance: ------------- **March 31, 2008**
Camera-Ready papers Due  ------------ **April 17, 2008**

## Workshop Organizers

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## Technical Program Committee:

All submitted papers will be rigorously reviewed by the session technical program committee members.

(International Program Committee to be announced shortly.)

If you have any questions about conference paper submission, please contact conference Program Chair: Waleed W. Smari, Dept. of Electrical and Computer Engineering, University of Dayton, 300 College Park, Dayton, OH 45469-0226, USA, Voice: (937) 229-2795, Fax: (937) 229-4529, Email: Waleed.Smari@notes.udayton.edu. For information about the HPCS conference in general, please contact the General Chairs or consult the conference web site at http://cisedu.us/cis/hpcs/08/.

The Multi Conference web site is at http://www.scs-europe.net/conf/ecms2008/.